REMARKS/ARGUMENTS

The Office Action mailed August 25, 2004, has been received and reviewed. Claims 1 through 8 are currently pending in the application. Claims 1 through 8 stand rejected. Applicants have amended claim 1, and respectfully request reconsideration of the application as amended herein.

Preliminary Amendment

Applicants' undersigned attorney notes the filing herein of a Preliminary Amendment on October 24, 2003, which filing was not acknowledged in the outstanding Office Action. Should the Preliminary Amendment have failed for some reason to have been entered in the Office file, Applicants' undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,444,663 to Furuno et al.

Claims 1 through 6 and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Furuno et al. (U.S. Patent No. 5,444,663). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants assert that the Furuno reference does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of amended independent claim 1, and claims 2-8 depending therefrom, because the Furuno reference does not describe, either expressly or inherently, the identical inventions in as complete detail as are contained in the claims.

The Office Action alleges:

> With regard to claim 1, Furuno discloses a memory device comprising: a memory array (fig. 1, MARY) for storing at least one data bit and configured to electrically

operate from a power supply voltage (fig. 1, Vpp); and a circuit (fig. 2, Voltage Follower) configured to receive an external reference voltage (fig. 2, Vref) and generate in response thereto an internal reference voltage (fig. 2, Vc) independent of the power supply voltage, **the internal reference voltage for accessing and evaluation the at least one data bit in the memory array** (col. 8, line 29-59). (Office Action, p. 2; emphasis added).

Applicants respectfully disagree that the Furuno reference anticipates Applicants' invention as claimed in amended independent claim 1 which reads:

> 1. A memory device, comprising:
> a memory array for storing at least one data bit and configured to electrically operate from a power supply voltage; and
> a circuit configured to receive **an external reference voltage as generated external to the memory device** and generate in response thereto an internal reference voltage independent of the power supply voltage, **the internal reference voltage for accessing and evaluating a logic state of the at least one data bit in the memory array.** (Emphasis added.)

In contrast, the Furuno reference discloses:

> "FIG. 1 is a block diagram of EPROM embodying the present invention. FIG. 2 is a block diagram illustrating **the voltage conversion circuit CONV of FIG. 1.**" (Col. 2, lines 30-33; emphasis added).
>
> "FIG. 2 is a block diagram of a voltage conversion circuit embodying the present invention. **A reference voltage generating circuit forms a reference voltage Vref.** The reference voltage Vref is a constant voltage Vc corresponding to **the operating voltage Vcv** at about 3 V." (Col. 8, lines 29-34; emphasis added).
>
> "The internal constant voltage **Vc is supplied to a supply voltage switch** . . . [t]he supply voltage **Vcc supplied from the outside is also input to the supply voltage switch.**" (Col. 8, lines 37-40; emphasis added).
>
> "When the supply voltage Vcc supplied from the outside is relatively as high as about 5V, the **supply voltage switch outputs the internal constant voltage Vc as the internal operating voltage Vcv** and when it is relatively as low as about 3V, the **supply voltage switch directly outputs the supply voltage Vcc supplied from the outside in place of the internal constant voltage Vc as the operating voltage Vcv.**" (Col. 8, lines 45-52).

Clearly in direct contradiction to Applicants' invention as claimed, the Furuno reference discloses (i) a reference signal Vref generated internal to the memory device (as opposed to Applicants' claimed invention of "an external reference voltage as generate external to the

memory device") and (ii) a "Vc" output of the voltage follower wherein "the supply voltage switch outputs the internal constant voltage Vc as the internal operating voltage Vcv" (as opposed to Applicants' claimed invention of an "internal reference voltage for accessing and evaluating a logic state of the at least one data bit in the memory array").

Specifically, the Furuno reference in FIG. 1 illustrates the CONV element (detailed in FIG. 2) to include **only** a single input, namely Vcc. Clearly, the CONV element as detailed in FIG. 2 does not and cannot be "configured to receive an external reference voltage as generated external to the memory device" as claimed in Applicants' amended independent claim 1. Regarding the Furuno references use of the voltage follower's output signal Vc, such a signal is used as the "operating voltage" and is not therefore used as a reference signal "for evaluating a logic state" as claimed by the Applicants' amended independent claim 1.

Therefore, Applicants' amended independent claim 1, and claims 2-8 depending therefrom, are not anticipated by the Furuno reference under 35 U.S.C. § 102. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,444,663 to Furuno et al. in View of U.S. Patent No. 6,124,704 to Annema

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Furuno et al. (U.S. Patent No. 5,444,663) in view of Annema (U.S. Patent No. 6,124,704). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on

applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 7 is improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Regarding claim 7, which depends from amended independent claim 1, Applicants sustain the above-proffered arguments that Furuno does not teach, disclose or motivate Applicants' invention as claimed in amended independent claim 1. The Office Action introduces the Annema reference and alleges:

> With regard to claim 7, Furuno, as applied in prior rejection, disclose all claimed subject matter except wherein the circuit comprising a plurality of voltage followers serially coupled to receive the external reference voltage and generate in response thereto the internal reference voltage. However, Annema discloses a circuit comprising a plurality of voltage followers serially coupled (fig. 4, VF) to receive the external reference voltage (Vrft) and generate in response thereto the internal reference voltage (Vrft) and generate in response thereto the internal reference voltage (Vrf) (col. 4, line 10-39). (Office Action, pp. 3-4).

Even assuming arguendo, that the Annema reference teaches serially configured voltage followers, neither Furuno nor Annema teach, disclose or motivate Applicants' invention as claimed, namely:

> A memory device, comprising:
> a memory array for storing at least one data bit and configured to electrically operate from a power supply voltage; and
> a circuit configured to receive **an external reference voltage as generated external to the memory device** and generate in response thereto an internal reference voltage independent of the power supply voltage, **the internal reference voltage for accessing and evaluating a logic state of the at least one data bit in the memory array.** (Emphasis added.)

Therefore, Applicants respectfully request that the rejection of dependent claim 7 be withdrawn.

ENTRY OF AMENDMENTS

The amendments to claim 1 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1-8 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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